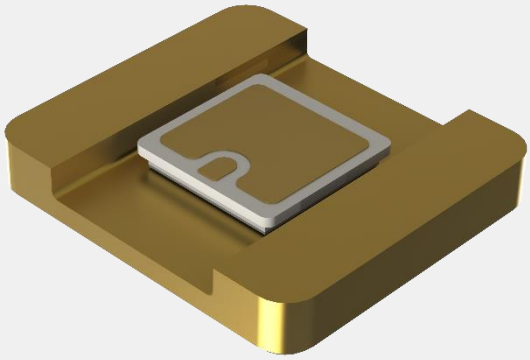
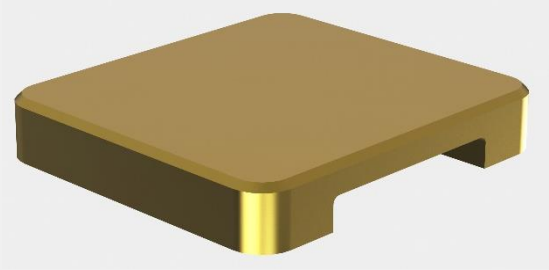
Mission Power

QuickFET™

1200-1700V SiC Package with low inductance & double-side cooling





Features

- Exceptional power density
- Low parasitic inductance
- Double-side cooling
- Low profile design
- High current capability
- High temperature operation

Benefits

- High efficiency
- Minimized EMI
- Optimized thermals
- Board space reduction
- Less device paralleling

Applications

- Electric vehicle drives & chargers
- Solid-state transformers
- Dual-active bridge
- Motor drives
- Inverters
- Power Supplies

Our Advantage

- Higher voltage than other low-inductance packages
- Ability to customize solution for preferred SiC die
- Easier to mount than bare-die
- No temperature limitations other than die junction temperature

Configuration

SiC bare die is sandwiched between two components that have Coefficients of Thermal Expansion (CTE) that are matched to the device. The joints employ double-sided sintering – a cutting edge approach for die attachment that eliminates wire-bonding. This allows the device to operate with high reliability and give maximum performance.

Performance - Inductance

Inductance is minimized by keeping drain and source conductors close to each other. More importantly, the device is configured such that board layout can be accomplished with lower inductance than any similar device. If the drain is on one layer of the board and the source is on another layer, the overall parasitic inductance is minimized.

Performance - Thermal

The package has high thermal conductivity spreading out the heat and allowing double-sided cooling. Further, because all parts of the device are solderable with gold plating, heat conducting structures can be attached by soldering.

Mounting flexibility

Configuration is compatible with double-sided mounting of devices allowing unique circuit configurations. Half-bridge topologies can be built with switches on opposite sides of two-layer board directly opposite of each other. This configuration minimized overall inductance and enables higher switching speeds on some multi-level topologies.

Manufacturing

QuickFET™ parts are designed to be used in a vacuum potted assembly. Creepage/clearance dimensions between drain and source are insufficient for almost any application. Solid insulation in the form of a high-quality vacuum potted resin is necessary for operation. Potting is often required for assemblies where this would be used, allowing the size of the QuickFET™ package to be minimized while maximizing performance.